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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/812,323	03/29/2004	Ahmad R. Ansari	NEC0217C2US	2725

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EXAMINER	
ELLIS, RICHARD L	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/812,323	ANSARI, AHMAD R.	
	Examiner	Art Unit	
	Richard Ellis	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *28-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *28-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/29/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Claims 28-41 are presented for examination.

2. The text of those sections of Title 35, US Code not included in this action can be found in a prior Office Action.

3. The numbering of claims is not accordance with 37 CFR § 1.126. The original numbering of the claims must be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When claims are added, except when presented in accordance with 37 CFR § 1.121(b), they must be renumbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 39-42 have been renumbered 38-41, respectively.

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The current title is imprecise.

5. 35 USC § 101 reads as follows:

> "Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter or any new and useful improvement thereof, may obtain a patent therefore, subject to the conditions and requirements of this title".

6. Claims 28, 30 and 33 are rejected under 35 USC § 101 because the claimed invention is directed to non-statutory subject matter.

7. Claims 28, 30 and 33 are nonstatutory for merely manipulating data without tying such manipulation of data to a useful, concrete, and tangible result. Claims 28, 30 and 33 claim the mere manipulation of data, specifically the mathematical calculations of multiplication, subtraction, and addition. The claims do recited any disclosed tangible result from the action of multiplication, subtraction, and addition. The claim is directed merely to a disembodied mathematical algorithm without linking that algorithm to a disclosed tangible result.

8. Claims 28, 30 and 33 are nonstatutory for claiming a mathematical algorithm, per. se. Claims 28 and 30 are method claims, and claim 33 is a computer readable medium claim, however, the only recited method steps are the steps of multiplication, subtraction, and addition. As written, the claims are directed to a mathematical algorithm. Mathematical

algorithms are non-statutory subject matter.

9. Finally, the mathematical algorithm presented in claims 28, 30 and 33 are not claimed as connected or tied to any form of practical application. Accordingly, these claims are so broad so as to cover any and all uses of this mathematical algorithm, used in any and all practical applications, that perform multiplication, addition, and subtraction. The result of this breadth is that the claim effectively preempts every substantial practical application of the abstract idea of multiplication, addition, and subtraction and therefore additionally become a claim to the mathematical algorithm itself. These claims therefore would, if they were to issue as a patent, preempt the judicial exception against claiming of mathematical algorithms. Therefore, claims 28, 30 and 33 are non-statutory claims.

10. Claims 28-39 all contain a limitation of determining an ending address based on the phrase "memory bus data width". However, the phrase "memory bus data width" does not exist at any point within the specification such than an explicit applicant intended definition of "memory bus data width" can be found. Accordingly, the plain meaning of the phrase must be determined. In order to determine the plain meaning intended by this phrase, the specification must be consulted.

In the current specification, the phrase "memory bus" occurs twelve (12) times, at pg. 22 line 8, pg. 26, lines 3, 4, 11, 12, 13, 14, 16, 21, and 24, pg. 27 lines 8 and 19 and the phrase "data width" occurs twelve (12) times at pg. 13 lines 13 and 25, pg. 14 lines 2, 4, and 5, pg. 16 line 1, pg. 17 line 23, pg. 19 line 6, pg. 20 line 7, pg. 26 lines 24 (two occurrences), and pg. 27 line 1.

In all cases of the usage of the term "data width" in the specification, such usage is in terms of the size of a data value to be operated upon by the computer system. E.g., see pg. 20 lines 5-10, where "data width" defines whether the instruction MVT instruction operates upon data values ranging in size from one byte each to 8 bytes each in size. Furthermore, at pg. 26 line 9, the following statement is found: "*or if the width of the data entries is equal to the width of memory bus 224*". This statement is further evidence that use of the term "data

width" within the specification is relating to the size of the data being operated upon by the system because it presents a clear distinction between "width of the data" vs. "width of the memory bus". As is seen from the next sentence: "*However, for streams whose data elements are smaller than the width of memory bus 224 ...*" the specification clearly shows that the data element size (data width) is independent of the memory bus size (width of memory bus).

Therefore, from this usage of "data width" in the specification, it is clear that the intended meaning of "data width" is the size of the data that is being operated upon. Therefore, the plain meaning of "memory bus data width" would be the size of the data that is being operated upon by the memory bus (i.e., being transferred across the memory bus).

11. Claims 28-29, 31-32 and 39-40 are rejected under 35 USC § 102(b) as being clearly anticipated by Smith, U.S. Patent 5,895,501.

Smith was cited in applicant's information disclosure statement filed March 29, 2004.

Smith taught (e.g. see figs. 1-4) the invention as claimed (as per claim 28), including a data processing ("DP") system comprising:

A. issuing (col. 5 lines 48-60) an instruction (col. 3 lines 43-46) to transfer data between a memory and a processor (col. 12-13 lines 12-13), wherein the instruction comprises a starting address of the data to be transferred (col. 6 lines 56-60);

B. determining an ending address of the data to be transferred from the starting address and a memory data bus width (col. 7 lines 58-62, where the "vector length" is the size of the data being operated upon by the memory bus because it defines the size of the vector being loaded or stored).

12. As to claim 29, Smith taught generating an address exception when it was determined that the data to be transferred crossed a page boundary of a page in the memory (col. 7 line 58 to col. 8 line 8).

13. As to claim 32, Smith taught initiating a data transfer between the memory and the processor (col. 7 lines 11-15); and,

interrupting the data transfer in response to generating the address exception (col. 7 lines 50-

65).

14. As to claim 31, Smith taught transferring the data to be transferred between the memory and the processor via a burst transfer (col. 6 lines 55-63).

15. As to claims 39-40, they do not teach or define above the invention claimed in claims 28-29 and 31-32 and are therefore rejected under Smith for the same reasons set fourth in the rejection of claims 28-29 and 31-32, supra.

16. Claims 30 and 41 are rejected under 35 USC § 103 as being unpatentable over Smith, U.S. patent 5,895,501. Additionally, Andrew Koenig, *C Traps and Pit Falls*, 1988 is cited as evidence showing the calculation of the size of a vector in memory.

17. As to claims 30 and 41, applicant has not only claimed a mere mathematical algorithm resulting in a claim to non-statutory subject matter, but applicant has also claimed the basic, obvious, method of calculating the address of the last one of a list of plural elements, each of size X, with a stride between elements of size Y. As seen from Koenig, on pg. 28, to calculate the size of a vector in memory one multiplies the number of elements by the individual size of each element ("sizeof(calendar) is 372 (31x12) times sizeof(int)"). This calculation provides the total size of the vector in memory. If this size is then summed with the starting address, the result will obviously be the next address past the vector. Therefore, by simple mathematical deduction, in order to locate the address of the final element in memory, one simply calculates the size of the vector minus one element. This value, when summed with the starting address will then refer to the final element in memory. As applicant's claims recite finding the "ending address of the data" applicant is locating the address of the end (last one) of the data, and not the address of the next location past the data set. Therefore, through simple mathematical deduction, it would have been obvious to one of ordinary skill in the art at the time the invention was made to subtract one from the length before multiplying by the width and stride and length in order to arrive at the address of the last one of the data elements.

18. Claims 33-34 and 36-38 are rejected under 35 USC § 103 as being unpatentable over

Smith, U.S. Patent 5,895,501, in view of Tanenbaum, *Structured Computer Organization*, 1984.

19. Smith taught the invention of claims 33-34 and 36 as detailed in the rejection of claims 28-29 and 31-32, supra. Smith did not teach that the invention was in the form of a computer readable medium. However, Tanenbaum taught that "hardware and software are logically equivalent" (pg. 11) and "Any operation performed by software can also be built directly into the hardware and any instruction executed by the hardware can also be simulated in software" (pg. 11). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to have implemented Garde et al.'s system as a storage medium storing instructions for causing a processor to perform the recited steps because of Tanenbaum's teaching that the decision to put certain functions in hardware vs. software is "based on such factors as cost, speed, reliability, and frequency of expected changes."

20. As to claim 37, Smith taught initiating a data transfer between the memory and the processor (col. 7 lines 11-15); and,
interrupting the data transfer in response to generating the address exception (col. 7 lines 50-65).

21. As to claim 38, Smith taught performing a burst transfer of the stream of vector data from the memory directly to a vector buffer (fig. 1, 120) of the processor (col. 6 lines 55-59), the burst transfer bypassing a data cache of the processor (fig. 1 shows the vector registers 120 connected directly to memory without cache, so the burst vector transfer bypasses the caches (140, 160, 170).

22. Claim 35 is rejected under 35 USC § 103 as being unpatentable over Smith, U.S. Patent 5,895,501, in view of Tanenbaum, *Structured Computer Organization*, 1984. Additionally, Andrew Koenig, *C Traps and Pit Falls*, 1988 is cited as evidence showing the calculation of the size of a vector in memory.

23. As to claim 35, they do not teach or define above the invention claimed in claims 30 or 41 and are therefore rejected under Smith in view of Tanenbaum with Koenig cited as evidence

for the same reasons set fourth in the rejection of claims 30 or 41, supra.

24. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) days from the mail date of this letter. Failure to respond within the period for response will result in **ABANDONMENT** of the application (see 35 USC 133, MPEP 710.02, 710.02(b)).

25. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Richard Ellis whose telephone number is (571) 272-4165. The Examiner can normally be reached on Monday through Thursday from 7am to 5pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Eddie Chan, can be reached on (571) 272-4162. The fax phone number for the USPTO is: (703)872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (571) 272-2100.

Richard Ellis
September 5, 2006

RICHARD L. ELLIS
PRIMARY EXAMINER